Designing a Second Order Generalized Integrator Digital Phase Locked Loop based on a Frequency Response Approach

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***Abstract*—This paper presents a Digital Phase-Locked Loop (PLL) based on the Second Order Generalized Integrator (SOGI). The PLL structure, as well as the SOGI, are carefully described. The integrators of the SOGI are explained in detail in order to emphasize the elimination of an algebraic loop found in continuous time domain PLLs. The main contributions of this paper are to present the design of PLL entirely in z-domain and to present an easy, fast and accurate way to implement a digital PLL based on the SOGI structure. The digital SOGI PLL is implemented in the digital signal processor TMS320F28335. Experimental and simulation results show the efficacy of the digital SOGI PLL to keep synchronized with grid voltage at frequencies 50 and 60 Hz.**

***Index Terms*-- Phase locked loops, SOGI, backward integrator, forward integrator.**

I. INTRODUCTION

PLLs play an important and indispensable role in electric power system applications whose synchronization with the electrical grid is a strict requirement. Synchronization is mandatory due to a variety of reasons, such as having a synchronized current and voltage at the output terminals of a grid-connected inverter, having the control strategy running in a synchronized reference frame as *dq* coordinates, having a satisfactory power flow between two or more distributed generators and maintaining power flow references provided by an upper layer energy management supervisory control [1]–[3].

For most applications, a PLL generates a signal synchronized with the grid voltage [4]–[7]. Such a signal is used for specific control purposes. Therefore, a PLL must be robust when the frequency of the grid deviates from its nominal value, and also reliable against harmonic distortions. A PLL must track deviations and keep the generated signal always synchronized with the grid voltage. It is a fact that, frequency tracking is not maintained by most types of PLLs. A PLL can be conceived in several ways; the most common structures are (*i*) the elementary, (*ii*) in-quadrature, (*iii*) Park transformation, (*iv*) inverse Park transformation [8]–[10] (*v*) SOGI [11]–[15] and (*vi*) Kalman Filter based ones [16], [17]. Each one has its features, efficacy, advantages and disadvantages.

The SOGI PLL deserves special attention due to its ability to cancel the double-frequency component commonly found in PLLs and also the ability to operate in suited range of frequency [10]. The SOGI part of the PLL creates two signals named in-phase and in-quadrature. They are orthogonal from each other and the in-phase signal is synchronized to the grid voltage. These signals are free of distortions that are eventually found in the grid voltage.

PLL based on SOGI have been constantly presented in the literature [18]–[22]. However, most of them explain the PLL in continuous time domain. The discretization of the PLL usually falls to the readers. The digital implementation of a SOGI PLL is not trivial because the SOGI part may lead to algebraic loop, preventing the PLL to work on its normal operation and there are resetting mechanisms to be implemented for a reliable and functional operation. A variety of power electronics applications needs a PLL on their control strategy [23]–[30].

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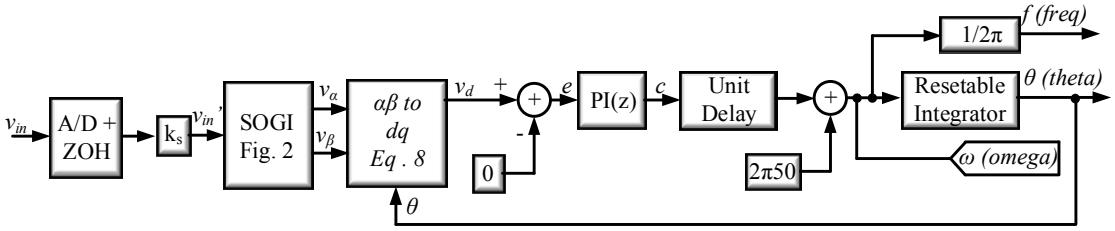

Figure 1. Simplified diagram of the Digital PLL

In this paper it is presented how to properly design a SOGI Digital PLL. The PLL structure as well as the SOGI are clearly described. It is explained how integrators of the SOGI can properly eliminate an algebraic loop. A resettable integrator is discussed in detail. The implementation of a Digital SOGI PLL using a DSP TMS320F28335 is performed. Experimental results show the efficacy of the digital SOGI

PLL to keep synchronized with grid voltage at frequencies 50 and 60 Hz. The procedure described in this paper can retrofit to any microcontroller, microprocessor, or FPGA hardware-based control system.

II. THE DIGITAL PLL

Fig. 1 presents the simplified diagram of the digital PLL. A grid voltage is measured (v_{in}) and it passes through an Analog to Digital Converter (A/D) with Zero Order Holder (ZOH). This block is usually embedded in the analog input of a digital signal processor. Later, the signal is multiplied by the gain *ks*. This gain is to compensate the sensor gain. Its value is the inverse of the sensor gain. The resulted signal is then applied in the SOGI block, which will be described in Fig. 2. The output signals of the SOGI block are in-phase and in-quadrature signals. They are orthogonal related to each other. The in-phase signal is synchronized with the grid voltage.

The in-phase and in-quadrature signals are transformed to *dq*-rotating reference frame. The v_d signal is compared to zero, creating the errors signal (*e*), which in turn passes through the PI controller. The PI output signal is delayed by one sample in order to avoid algebraic loop. The value of the fundamental angular frequency is added to the PI output signal. At this point the PLL has obtained the fundamental angular frequency of its input signal, which in this case is the grid voltage. By dividing the angular frequency by 2π, the PLL supplies the fundamental frequency in Hertz. The angular frequency is sent to a *goto* tag because it is used in the SOGI block. The fundamental angular frequency is integrated through a resettable integrator, obtaining the phase signal *theta*. The *theta* signal is sent to the to *dq* conversion block. Even though the PLL block diagram does not show, the RMS value of the grid voltage could be obtained by computing the magnitude of the in-phase and in-quadrature signals.

A. SOGI

Fig. 2 presents the simplified diagram of the SOGI. The SOGI is responsible for creating the in-phase and in-quadrature signal from the grid voltage. The SOGI block uses the angular frequency before computing the integrator. It is important to highlight that the angular frequency comes from Fig. 1. The gain *k* is the SOGI gain and its value has an important role in the behavior of the PLL. The SOGI is able to eliminate the double-frequency components that appears in the measured fundamental frequency. The low-pass filter is used to reduce the noise which may appear in the error signal. The SOGI uses two integrators. These integrators need special attention because one is based on a forward integration method while the other is based on backward integration. This is necessary to avoid algebraic loop in the SOGI block. They are discussed in the next section.

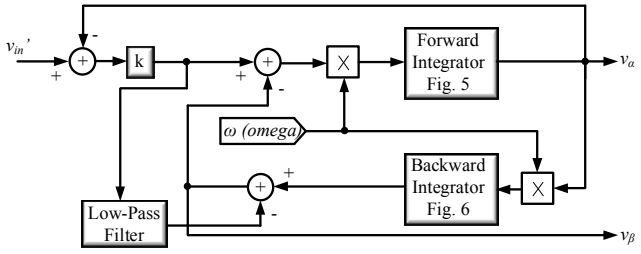

Figure 2. Simplified diagram of the SOGI

The SOGI structure in *s*-domain is defined by (1) [11].

$$SOGI(s) = \frac{\omega s}{s^2 + \omega^2} \tag{1}$$

ω is the fundamental angular frequency, known also as resonant frequency. The closed-loop transfer function for the *alpha* and *beta* voltages are given by (2) and (3), respectively.

$$H_\alpha(s) = \frac{v_\alpha(s)}{v(s)} = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{2}$$

$$H_\beta(s) = \frac{v_\beta(s)}{v(s)} = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{3}$$

Fig.3 presents the bode diagrams for equations (2) and (3), valid for $k = 0.25$ and $\omega = 2\pi 60$. Notice that the magnitude response for both $H_\alpha(s)$ and $H_\beta(s)$ present a single point where the magnitude is 0 *dB*, which is approximately 377 rad/s (60 Hz). All the remaining frequencies are attenuated. This implies that the input voltage of the PLL may contain noise and distortion and the frequency is estimated anyway. The SOGI acts as a low-pass filter, supplying later a clean signal to the PLL.

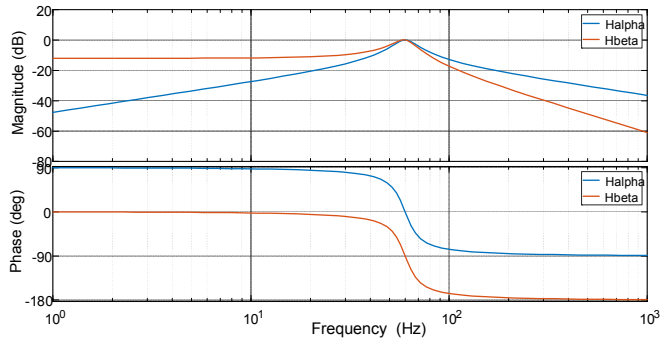

Figure 3. Bode diagrams for equations (2) and (3).

The discretization of (2) and (3) are obtained by applying the Bilinear transform in these equations. Therefore, the discrete closed-loop transfer function for the *alpha* and *beta* voltages are given by (4) and (5), respectively. Other methods of discretization might be applied. For each method, the frequency response will be slightly different. In [14] there are descriptions of such methods.

$$H_\alpha(z) = H_\alpha(s)\Big|_{s=\frac{2(z-1)}{t_s(z+1)}} \tag{4}$$

$$H_\beta(z) = H_\beta(s)\Big|_{s=\frac{2(z-1)}{t_s(z+1)}} \tag{5}$$

The result of applying the Bilinear transform are given by (6) and (7). They are the discrete transfer function for the *alpha* and *beta* voltages.

$$H_\alpha(z) = \frac{g_1\left(z^2-1\right)}{m_1 z^2 + m_2 z + m_3} \tag{6}$$

$$H_\beta(z) = \frac{g_2\left(z^2+2z+1\right)}{m_1 z^2 + m_2 z + m_3} \tag{7}$$

where

$$\begin{aligned} g_1 &= \frac{2k\omega}{t_s} \\ g_2 &= k\omega^2 \\ m_1 &= \frac{4}{t_s^2} + \frac{2k\omega}{t_s} + \omega^2 \\ m_2 &= 2\omega^2 - \frac{8}{t_s^2} \\ m_3 &= \frac{4}{t_s^2} - \frac{2k\omega}{t_s} + \omega^2 \end{aligned} \tag{8}$$

Fig.4 presents the bode diagram for the discrete closed-loop transfer function of *alpha* and *beta* voltages. The Bode diagram is very similar to the *s*-domain Bode diagrams shown in Fig.3, except for high frequencies.

After computing the *alpha* and *beta* voltages, the *αβ* to *dq* transformation is applied. According to Fig.1, only the *d*-axis

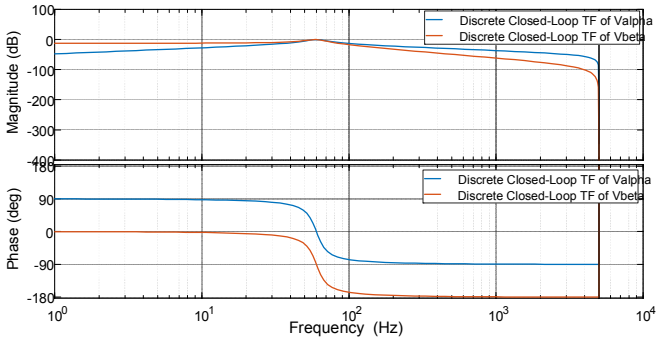

Figure 4. Bode diagram for the discrete closed-loop transfer function of *alpha* and *beta* voltages.

is used after the transformation. Therefore, the *αβ* to *dq* transformation is given by (8).

$$v_d = v_\alpha \cos(\theta) + v_\beta \sin(\theta) \tag{9}$$

B. Forward Integrator

Fig.5 presents the block diagram of the forward integrator. The integrator is a third-order IIR filter structure with constant coefficients a_1, b_1, b_2 and b_3 and whose time-domain expression is given by (9).

$$\begin{aligned} out(n) &= a_1 out(n-1) \\ &+ \frac{t_s}{12}\left[b_1 in(n-1) + b_2 in(n-2) + b_3 in(n-3)\right] \end{aligned} \tag{10}$$

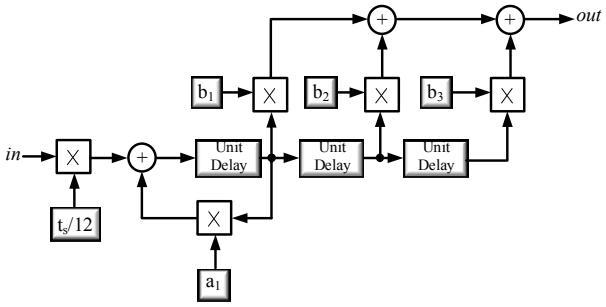

Figure 5. Block diagram of the Forward Integrator.

C. Backward Integrator

Fig.6 presents the block diagram of the backward integrator. The integrator is also a third-order IIR filter structure with constant coefficients b_4, b_5 and b_6. The time-domain expression is given by (10).

$$\begin{aligned} out(n) &= a_1 out(n-1) \\ &+ \frac{t_s}{12}\left[b_1 in(n-1) + b_2 in(n-2) + b_3 in(n-3)\right] \end{aligned} \tag{11}$$

$$\begin{aligned} out(n) &= out(n-1) \\ &+ \frac{t_s}{12}\left[b_4 in(n-1) + b_5 in(n-2) + b_6 in(n-3)\right] \end{aligned} \tag{12}$$

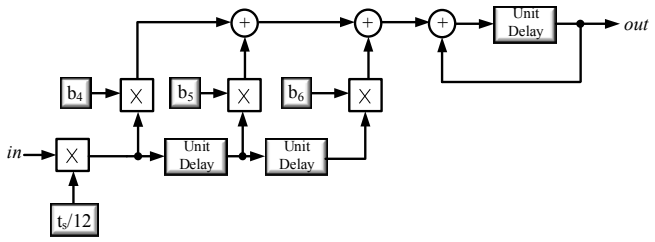

Figure 6. Block diagram of the Backward Integrator.

D. *Resetable Integrator*

The resettable integrator of the PLL shown in Fig.1 is necessary to guarantee that the theta signal varies from 0 to 2π. Therefore, the resettable integrator must operate in such a range. The majority of simulators, such as Simulink and PSIM, has the resettable integrator as a common block, which can be used easily.

III. SIMULATED RESULTS

The PLL of Fig.1 was simulated in Matlab/Simulink. The system parameters of the PLL are given in Table I.

TABLE I. SYSTEM PARAMETERS OF THE DIGITAL PLL

Parameter	**Value**
Coefficient a_1	1
Coefficient b_1	23
Coefficient b_2	-16
Coefficient b_3	5
Coefficient b_4	23
Coefficient b_5	-16
Coefficient b_6	5
Proportional gain of the PI	0.3
Integral gain of the PI	13
SOGI gain (k)	1.4
Sensor gain compensation (k_s)	180
Sampling period (t_s)	1e-4

Fig.7 presents the input signal of the PLL measured right after the ADC+ZOH block. Initially, the input signal is clean sinusoidal. At t = 0.5s, noise is intentionally applied to the input signal in order to verify the behavior of the PLL.

Fig.8 presents the v_α, v_β and theta θ signals. The noise is still being applied at t = 0.5s. All three signal are free of noise, verifying the ability of the SOGI to filter the input signal as well as the PLL to work with input signal with noise. Fig.9a presents the frequency signal of the PLL. Initially, the frequency is equal to 60Hz.

At t=0.5, the noise is applied and the frequency signal presents an oscillatory behavior.

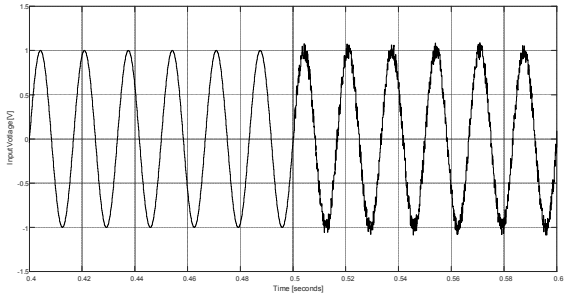

Figure 7. Input signal of the PLL measured right after the ADC+ZOH block.

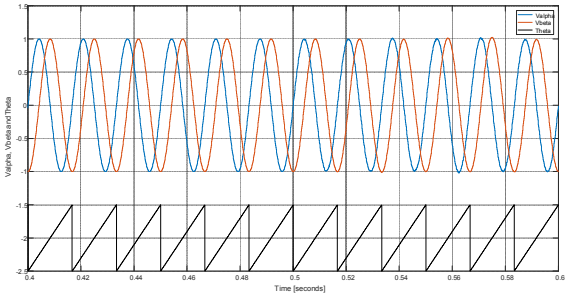

Figure 8. v_α, v_β and theta θ signals.

Even though such behavior, the performance of the PLL is not compromised, as observed in the previous figures. Fig. 9b presents results when the input signal has a third harmonic components. The amplitude of the third harmonic is 10% of the amplitude of the fundamental component. The valpha and vbeta signal has distortion. However, the theta signal is synchronized with the input signal.

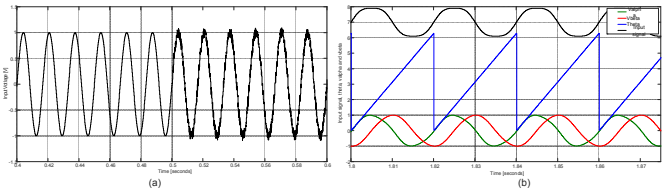

Figure 9. (a) Frequency signal of the PLL; (b) intput signal with harmonic distortion, theta signal, valpha and vbeta signals.

IV. EXPERIMENTAL RESULTS

The PLL of Fig.1 was experimentally verified in the Digital Signal Processor TMS320F28335 from Texas Instruments. A signal generator device was used to generate the input signal of the PLL. To visualize the digital variables in the oscilloscope, the Serial-Peripheral Interface of the DPS an external Digital-Analog Converter IC (MCP4922) were used. The system parameters are the same of those of Table I.

Fig.10 presents the input signal and the *theta* signal. The input signal is a 50 Hz sinusoidal waveform. The *theta* is synchronized with the input signal, showing the efficacy of the proposed PLL.

Fig.11 presents the input signal and the theta signal, but now the input signal is a 60 Hz sinusoidal waveform. The theta is also synchronized with the input signal. This result and

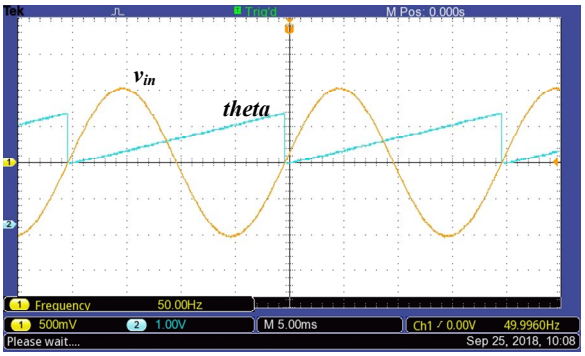

Figure 10. The synchronized theta signal for a 50Hz frequency input signal.

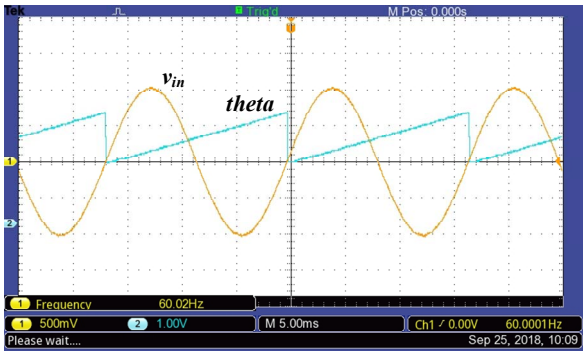

Figure 11. The synchronized theta signal for a 60 Hz frequency input signal.

the previous shows that the PLL works satisfactory for input signal with frequencies 50 and 60 Hz.

Fig.12 presents the measured frequency and the theta signal for frequency step in the input signal. The frequency varies from 50 to 60 Hz. These values of frequencies can be observed in the theta signal. The measured frequency does not present the commonly found double-frequency oscillation. Moreover, the measured frequency reaches its reference value (not shown) after the step. Even though a frequency variation from 50 to 60 Hz is not found in grid voltage, this scenario was verified experimentally in order to show the efficacy of the PLL to track variations in frequency. This variation may be considered the worst case.

Fig.13 presents the measured frequency and the theta signal for frequency step in the input signal. Now the frequency varies from 60 to 50 Hz. Similarly, to the previous case, the measured frequency reaches its reference value (not shown) without presenting an unpredictable behavior.

Fig.14 presents the input and output signal of the PLL for a frequency step from 60 to 50 Hz. The output signal is made by sin θ. Initially, the output signal is synchronized with the input signal. After the step, the output signal is synchronized again after approximately three cycles.

Fig.15 presents the input and theta signal for a phase step in the input signal. The input signal suffers a 45 degrees shift. The theta reaches synchronization with the input signal after approximately three cycles.

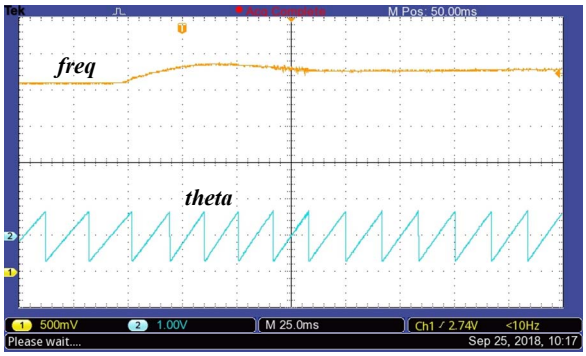

Figure 12. The measured frequency and theta signals for a frequency step from 50 to 60Hz.

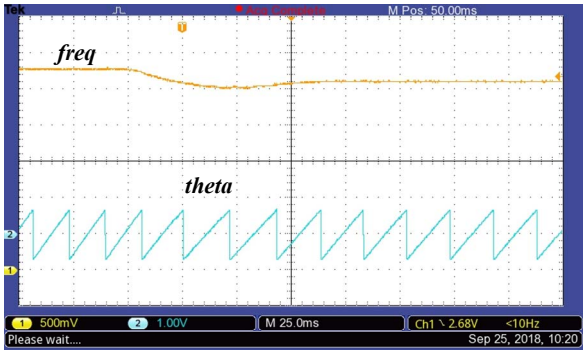

Figure 13. The measured frequency and theta signals for a frequency step from 60 to 50Hz.

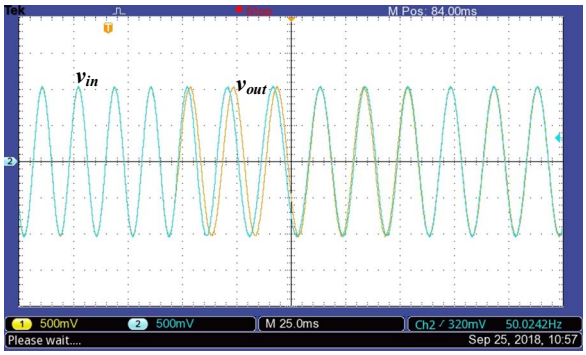

Figure 14. The input and output signal for a freq. step from 60 to 50 Hz.

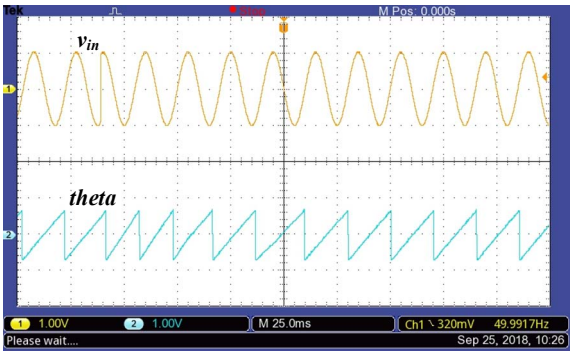

Figure 15. The input and theta signals for a phase step in the input signal.

V. CONCLUSIONS

This paper presented a Digital PLL based on the SOGI. The PLL structure as well as the SOGI were carefully described. The integrators of the SOGI were explained in detail in order to emphasize the elimination of algebraic loop found in continuous time domain PLLs. Simulation results showed that the SOGI has the ability to filter the input voltage. So, the PLL is able to work under distorted and noisly input signal. Experimental and simulation results showed the efficacy of the digital SOGI PLL to keep synchronized with grid voltage at frequencies 50 and 60 Hz. During transient verification, the PLL did not show unpredictable behavior. Therefore, the digital PLL presented in this paper is an attractive tool which ensures an easy, fast and accurate way to use digital PLL in electric power applications. The simulation files used in this research is freely available on the author's webpage **http://busarello.prof.ufsc.br**.

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