Understanding the time delay caused by digital control strategies and its model in the frequency domain

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1 Introduction

This tutorial explains the time delay caused by digital control strategies in power electronics applications as well as its representation in the frequency domain (s-domain). It is quite common to see a transfer functions in s-domain representing the delay caused by digital controls. Such a function comes from the Padé's approximation. This tutorial also explains how to properly account for the delay parameter in the transfer function.

2 Representing a delayed signal in time-domain

Figure 1 presents a time-domain signal consisting of a single pulse occurring at the instant t_0. Note that the variable on the x-axis is time (t), therefore the signal is represented by the function $x(t)$.

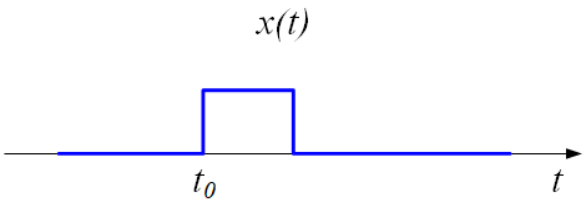

Figure 1: Time-domain signal consisting of a single pulse occurring at the instant t_0.

If, for any reason, the signal mentioned above is delayed, causing the pulse to occur at the instant t_d, the result is illustrated in Figure 2. Notice that the duration of the delay is represented by T_d, which is constant value.

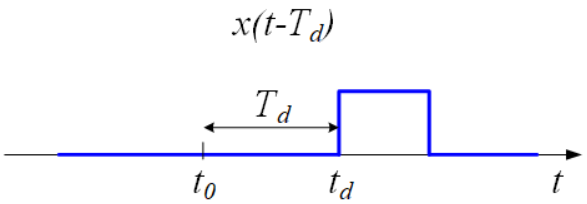

Figure 2: The same signal of the Figure 1, but now with the pulse occurring at t_d.

Considering the signals illustrated in Figures 1 and 2, we can conclude:

- the shape of the signal did not change;
- the signal is now described by the function $x(t - T_d)$.
- $t_d > t_0 > 0$)

3 Representing a delayed signal in frequency-domain

Since most linear controllers for power electronic applications are designed in the frequency domain, specifically the s-domain, the signals discussed in the previous section must be transformed to such a domain.

To transfer a signal from time-domain to the frequency-domain, the Laplace Transform is typically used. The formal definition and properties of the Laplace Transform are beyond the scope of this tutorial. Nevertheless, a very popular property is the Time Shifting.

The following pairs of equations show how the signals $x(t)$ and $x(t - T_d)$ are represented in the frequency domain through the Laplace Transform:

$$x(t) \Leftrightarrow X(s) \tag{1}$$

$$x(t - T_d) \Leftrightarrow X(s)e^{-sT_d} \tag{2}$$

With these equations, we can conclude:

- the delay in a signal of duration T_d appeared as e^{-sT_d} in the frequency domain.
- the term e^{-sT_d} represents a phase shift in the system, as will be observed later.

4 Using the Padé's approximation to replace e^{-sT_d}

As mentioned earlier, linear controllers are typically designed in the frequency domain (the s-domain). These controllers are later implemented on digital devices, such as microcontrollers or FPGA boards. Therefore, during the design process, it is very important to account for the delay introduced by the digital implementation. It's also important to note that, at some point, the controller will be discretized. However, the discretization process is beyond the scope of this tutorial, and it is assumed that the discretization has been performed correctly. A paper with rich content about discretization can be found in [1].

The representation in s-domain of the time delay caused by the digital implementation could be done by inserting a representative transfer function as shown in the block of Figure 3.

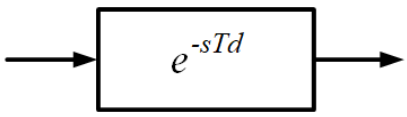

Figure 3: Representation in s-domain of the time delay caused the digital implementation.

The problem of using the block shown in Figure 3 is the fact that its transfer function is irrational, bringing complexities to the design process of the controllers.

So, one option is to use the Padé's approximation to replace the original transfer function.

The detailed derivation of Padé approximation equations is beyond the scope of this tutorial, but it is important to note that this approximation is derived from power series. Moreover, Padé's approximation can represent several function like the sine, Bessel and exponential function as a rational function of polynomials. The most commonly approximation used for the exponential function is the is the first-order approximation. Using high-order Padé's approximation is quite rare in power electronic applications, but one example can be found in [2].

Let's first examine the Padé's approximation in continuous-time domain. Equations (3) and (4) present the first and second-order Padé's approximation for the exponential function.

$$e^{-x\sigma} \approx \frac{1 - \frac{\sigma x}{2}}{1 + \frac{\sigma x}{2}} \tag{3}$$

$$e^{-x\sigma} \approx \frac{1 - \frac{\sigma x}{2} + \frac{\sigma^2 x^2}{12}}{1 + \frac{\sigma x}{2} - \frac{\sigma^2 x^2}{12}} \tag{4}$$

where σ is a constant.

Figure 4 shows the exponential function along with its first and second-order Padé approximations, with $\sigma = 0.1$. The x-axis represents time. From the figure, it is evident that the three functions coincide over a certain range of x. The smaller σ is, the larger the region of coincidence becomes. This is advantageous because, in digital control, we aim for a high sampling frequency, which results in a short sampling period and minimal time delay. Consequently, representing the delay using Padé approximations provides an accurate solution.

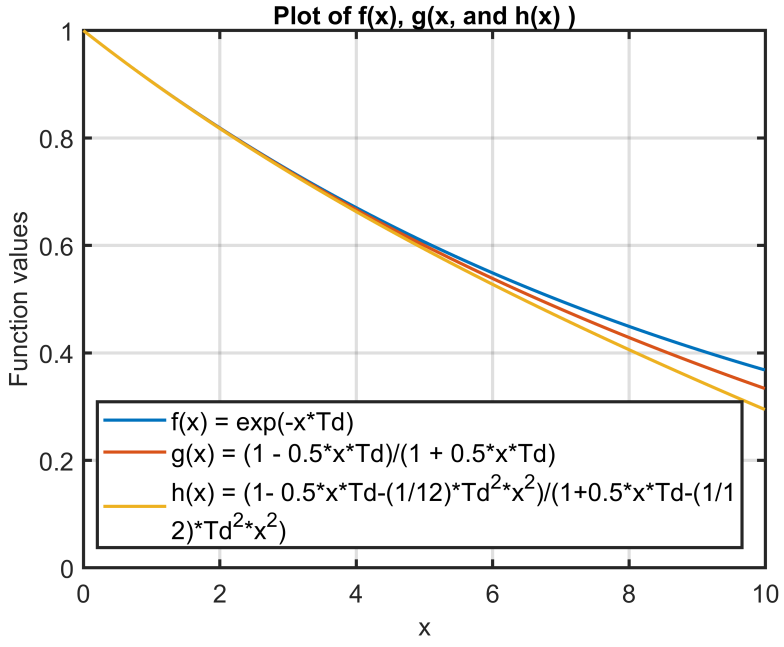

Figure 4: The exponential function and their first and second-order Padé's approximations.

Moving back to the s-domain, now we can replace the block shown in Figure 3 to that shown in Figure 6. As a result, the block shows the representation of the time delay by the first order Padé's approximation.

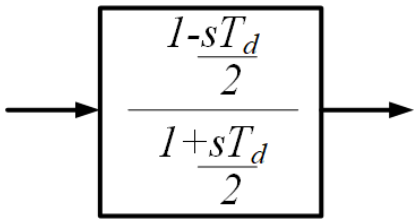

Figure 5: Representation of the time delay by the first order Padé's approximation.

To verify the effect that the inclusion of the above transfer function can cause in a control strategy, let's plot Bode diagrams of two transfer functions. The following transfer functions are taking as example. The first is a unitary transfer function and the second is the product of the unitary transfer function and the Padé's approximation.

$$FT(s) = 1 \tag{5}$$

$$FT_{delayed}(s) = FT(s).\frac{1 - \frac{sT_d}{2}}{1 + \frac{sT_d}{2}} \tag{6}$$

Figure 6 presents the frequency response of a unitary transfer function and its delayed version.

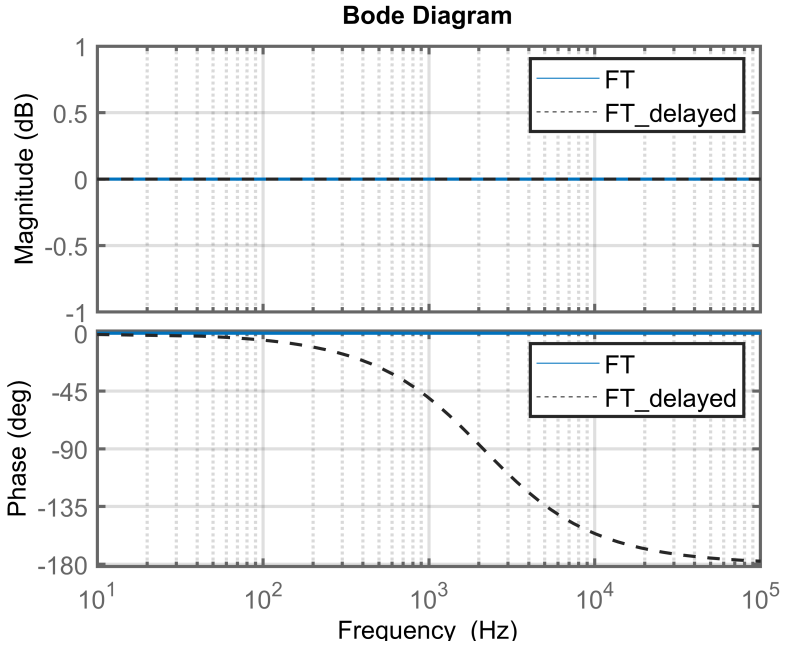

Figure 6: Frequency response of a unitary transfer function and its delayed version.

Looking at the frequency response that has just been plotted, we can conclude:

- in the Magnitude diagram, both responses are coincident. This was expected, since a time delay in a signal does not change its shape, as previously concluded.
- in the phase diagram, the delayed transfer function coincides with the unitary transfer function at low frequencies but begins to diverge significantly at higher frequencies.

- to plot these Bode diagrams, it was adopted $10kHz$ as sampling frequency and $T_d = 1.5T_s$, where T_s is the sampling period.
- if the sampling frequency increases, the time delay (T_d) decreases, resulting in a larger region of coincidence in the phase frequency response. This also leads to a larger region of overlap in the graphs shown in Figure 4.

5 What value to use in the constant T_d?

In the previous section, it was adopted $T_d = 1.5T_s$ [3, 4]. The 1.5 is actually $(1+0.5)T_s$, consisting of:

- $0.5T_s$ is attributed to the sampling and holding process, as illustrated in Figure 7. The figure presents the original signal (a sinusoidal signal in this case) and its sampled and held version. Additionally, the figure includes the *First Harmonic* representation. Within the microcontroller, only the sampled and held signal exists. Notice also that the first harmonic is delayed by half related to the sampling period. That's the reason the $0.5T_s$ is adopted. This is valid for any signal and any sampling frequency.
- $1T_s$ is attributed to the time required to compute the entire control algorithm. In summary, the control algorithm is a sequential process composed of the following steps: (i) sampling and holding the variables, (ii) computing the control algorithm, (iii) updating the PWM, and (iv) applying the result to the output. Therefore, one sampling period ($1T_s$) is the delay caused by the control algorithm.

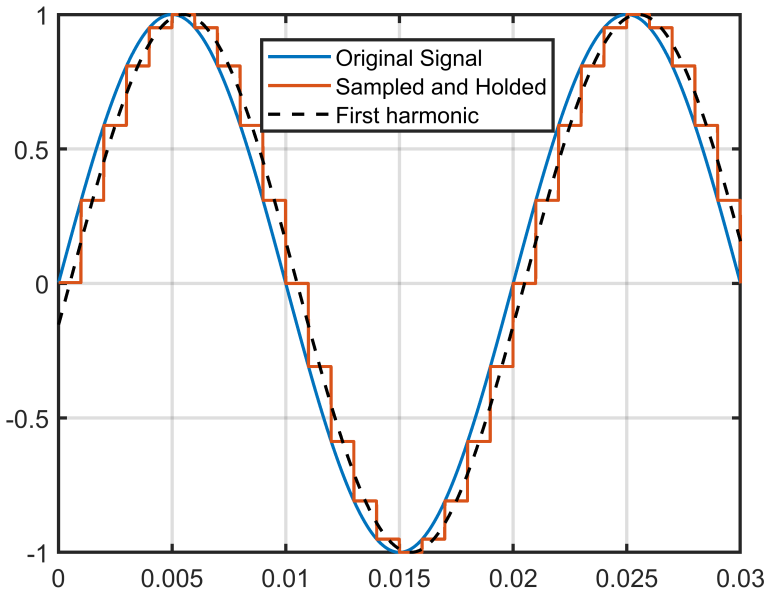

Figure 7: The original signal and its sampled and held version, as well as the first harmonic.

6 Final Considerations

As a final consideration, it is evident that selecting a high sampling frequency is beneficial, as it reduces the adverse effects of delays. However, a higher sampling frequency also limits the available time for executing the entire control algorithm.

Various techniques to mitigate the impact of delays are frequently discussed in the literature.

References

[1] A. G. Yepes, F. D. Freijedo, J. Doval-Gandoy, López, J. Malvar, and P. Fernandez-Comesaña, "Effects of discretization methods on the performance of resonant controllers," *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1692–1712, 2010.

[2] Y. Liao and X. Wang, "Impedance-based stability analysis for interconnected converter systems with open-loop rhp poles," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4388–4397, 2020.

[3] P. M. Simone Buso, *Digital Control in Power Electronics, 2nd Edition*, ser. Synthesis Lectures on Power Electronics. Springer Cham, 2015.

[4] M. L. W. Gene F. Franklin, J. David Powell, *Digital Control of Dynamic Systems*, ser. 3rd edition. Addison-Wesley, 1197.